

ABSTRACT OF THE DISCLOSURE

A broadcast receiver includes an input unit, a receiving unit, a control unit, a main memory, a demultiplexer unit, and a decoding unit. When a user switches on or resets the main power by operating the input unit, an operation signal (main-power switching-on signal or reset signal) is supplied to the control unit via a bus. The control unit reads, via the bus, the bit-rate value of transport stream data stored in a program area in a main memory. The control unit computes the optimal size of the FIFO buffer area based on the read bit-rate value and confirms it. The control unit reserves, in the main memory, the FIFO buffer area based on a result of the computation.

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